CLAIMS

What is claimed is:

1. A fixed point data generating circuit which receives a plurality of floating point data and which converts said plurality of floating point data into respective fixed point data, said fixed point data generating circuit comprising:

a reference data determining means which determines a reference floating point data from said plurality of floating point data;

an exponent part subtractor means which obtains a difference between each of values of exponent parts of said plurality of inputted floating point data and a value of an exponent part of said reference floating point data;

a shifting means which shifts a mantissa part of each of said floating point data by said difference obtained by said exponent part subtracting means; and

a bit extracting means which extracts a predetermined number of bits of said mantissa part shifted by said shifting means as fixed point data.

2. A fixed point data generating circuit as set forth in claim 1, wherein said reference data determining means is a maximum value detecting means which detects the maximum value among said plurality of floating point data and said reference floating point data is the maximum data among said plurality of floating point data.

3. A fixed point data generating circuit as set forth in claim 1,

wherein said reference data determining means is a minimum value detecting means which detects the minimum value among said plurality of floating point data and said reference floating point data is the minimum data among said plurality of floating point data.

4. A fixed point data generating circuit as set forth in claim 1, wherein said reference data determining means is an average value calculating means which calculates an average value of said floating point data and said reference floating point data is the average data of said plurality of floating point data.

5. A fixed point data generating circuit as set forth in claim 1, wherein said bit extracting means extracts bits as said fixed point data from a predetermined location.

6. A fixed point data generating circuit as set forth in claim 1, wherein, when an overflow occurs in said bits extracted by said bit extracting means as said fixed point data, said bits extracted are caused to represent the maximum value thereby.

7. A fixed point data generating circuit as set forth in claim 1, wherein, when an overflow occurs by shifting a mantissa part of each of said floating point data by said shifting means, shifted bits are caused to represent the maximum value thereby.

8. A fixed point data generating circuit as set forth in claim 1, wherein said fixed point data extracted by said bit extracting means is inputted to a Viterbi decoder.

9. A fixed point data generating circuit as set forth in claim 8, wherein location of bits extracted by said bit extracting means as said fixed point data is previously determined to be location having high decoding rate.

10. A method for generating fixed point data in which a plurality of floating point data are converted into respective fixed point data, said method comprising:

determining a reference floating point data from said plurality of floating point data;

obtaining a difference between each of values of exponent parts of said plurality of inputted floating point data and a value of an exponent part of said reference floating point data;

shifting a mantissa part of each of said floating point data by said difference between each of values of exponent parts of said plurality of inputted floating point data and a value of an exponent part of said reference floating point data; and

extracting a predetermined number of bits from said mantissa part shifted by said difference as fixed point data.

11. A method for generating fixed point data as set forth in claim 10, wherein said reference floating point data is the maximum data among said plurality of floating point data.

12. A method for generating fixed point data as set forth in claim 10, wherein said reference floating point data is the minimum data among said plurality of floating point data.

13. A method for generating fixed point data as set forth in

claim 10, wherein said reference floating point data is the average data of said plurality of floating point data.

14. A method for generating fixed point data as set forth in claim 10, wherein, in said extracting a predetermined number of bits from said mantissa part shifted by said difference as said fixed point data, said bits are extracted from a predetermined location.

15. A method for generating fixed point data as set forth in claim 10, wherein, in said extracting a predetermined number of bits from said mantissa part shifted by said difference as said fixed point data, when an overflow occurs in said bits extracted, said bits extracted are caused to represent the maximum value thereby.

16. A method for generating fixed point data as set forth in claim 10, wherein, in said shifting a mantissa part of each of said floating point data by said difference, when an overflow occurs by shifting a mantissa part of each of said floating point data, shifted bits are caused to represent the maximum value thereby.

17. A method for generating fixed point data as set forth in claim 10, wherein said fixed point data extracted in said extracting a predetermined number of bits from said mantissa part shifted by said difference is inputted to a Viterbi decoder.

18. A method for generating fixed point data as set forth in claim 17, wherein location of bits extracted in said extracting a

predetermined number of bits from said mantissa part shifted by said difference is previously determined to be location having high decoding rate.